Scan Ring Linker 14

SRL14-FG144

Revision 1.6.0

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Table of Contents

List of Figures

List of Tables

Confidential Information

Your Obligations

This document describes the features and capabilities of the SRL™. This information is supplied to you under Intellitech's website terms of use. You are obligated by this agreement not to disclose information about the design and operation of Eclipse, SRL, TEST-IP™ to any third parties. If you have any questions, please consult with your legal department or Intellitech Corporation.

Trademarks

SCAN RING LINKER 14

Features

- 14-Chain Scan Ring Linker with 3 master ports to allow TAP connectivity for multiple external controllers
- Configurable via Altera and Xilinx pods
- Support for TAPs with 2 different operating voltages
- Flexible control of scan paths where any ring can be turned on or off to achieve custom configurations for your boundary scan tests
- Supports TAP voltages of 1.5V, 1.8V, 2.5V, or 3.3V
- RoHS-compliant packaging option
- Provides link between an arbitrated master and any combination of 14 secondary scan paths
- External jumpers allow TAP controller to directly access a secondary scan chain without use of Intellitech tools. This feature allows other vendors' tools to directly control devices on a secondary scan chain. This feature is useful during processor emulation and FPGA debug.

Description

The Scan Ring Linker links multiple scan chains and controls the paths via one of three 1149.1 TAP master ports. Intellitech's Eclipse and Scan Executive software suites configure the SRL14 to link together any combination of the 14 scan chains during a test. The SRL14 allows one TAP controller to scan through multiple scan chains regardless of the location, operating voltage, or number of devices (Note: the number of devices connected to each scan chain may slow down speed to testing).

The SRL14 chip can operate in "pass-through" mode, allowing 3rd-party 1149.1-compliant TAP controller to directly connect to one of the 14 secondary scan rings without the use of any software. In "pass-through" mode, the SEL[3:0] input pins configure the SRL14 device to directly connect the user's TAP controller to the one selected chain. This feature allows the user to remove costly debug headers that consume valuable board real estate and to use only a single interface to connect to each of the JTAG chains.

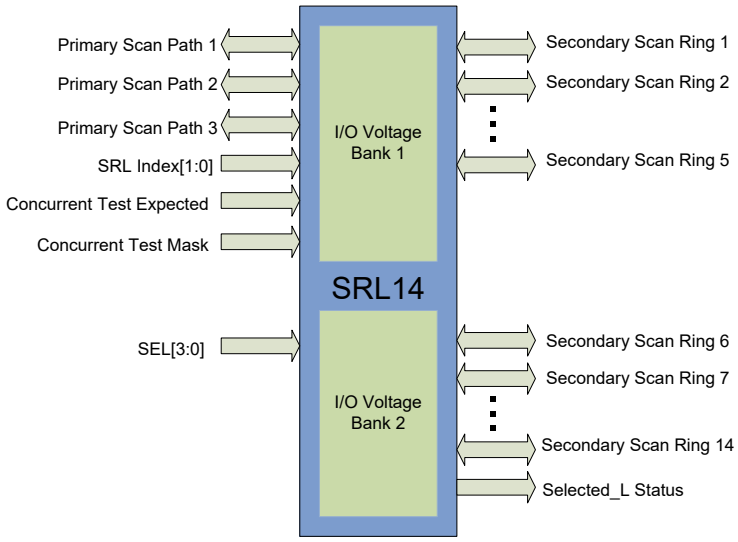


Figure 1: SRL Block Diagram

Capabilities

The SRL14 has 3 separate 1149.1 TAP interfaces that allow multiple masters to control the scan paths. Each chain can be accessed separately or in any combination of the 14 paths. The user can use Intellitech's Eclipse or Scan Executive software or, otherwise, use system jumpers to activate only the chain that is necessary for a test. The selected paths can be customized for each test in a multi-test environment.

The SRL14 allows secondary scan rings 6-14 to operate at a different bank voltage, allowing users to link scan chains of different operating JTAG voltages to create a single scan path. This simplifies testing by only having to connect to one chain rather than multiple chains at multiple voltages.

The SRL14 allows for the selection of a single JTAG chain without the use of Intellitech's Eclipse or Scan Executive software. By grounding one or more SEL[3:0] inputs, users can activate a single JTAG path while the other 13 chains remain disconnected from the active chain. This ability to enable a single ring is valuable for the debug of some systems with processors and FPGAs.

Using the SRL14 Device with Eclipse

The Eclipse reads in a database that describes how the 1149.1 standard is implemented within the SRL14. After parsing the database, Eclipse displays in the hierarchy window the connectivity of the devices on each secondary scan ring. This window describes the scan chains and gives the user the ability to turn on and off any of the output TAPs, referred to

as secondary scan rings (SSR's). This window also allows users to open spreadsheets for each of the devices within the chain, analyze system timing with Eclipse timing diagrams, and open Schematic Logic Probe (SLP), if applicable. A screen shot of the System Hierarchy window for a system using the Scan Chain Coupler is shown in **Error! Reference source not ound.**.

In the System Hierarchy window shown in **Error! Reference source not found.**, the plus and minus signs to the left of "srl14" allow users to expand the hierarchy, revealing the 14 output TAPs (labeled ssp0 through ssp13). The plus and minus signs to the left of each TAP allows users to expand the hierarchy of each separate scan chain. When describing the TAPs and the devices within them, Eclipse lists the last TAP or device in the chain first.

Users can turn scan chains on and off by double-clicking on the secondary scan path (in this example, i13 through i0). Rings that are not selected (i.e., turned off) are shown in italics. In the System Hierarchy window in **Error! Reference source not found.**, the first and seventh scan rings are the only scan rings turned on. If a scan ring is turned on, the ring must be fully connected in order for any of the scan rings to operate correctly since each "on" scan ring is put in a series chain within the SRL. If a scan ring is not connected, it should be turned off during testing or have TDI connected to TDO on the output TAP.

Scan Chain Hierarchy

The scan path hierarchy of the SRL14 chains is described in a Device Chain Description File (DCD). An example of a DCD file for a system that uses an SRL14 is shown in Appendix G: Example DCD File with SRL14. Once the DCD file is compiled with Eclipse, the SRL14's paths can be controlled to turn on a single chain, all chains, or any combination. The user can isolate testing to a single chain or perform system level testing on multiple chains without reconfiguration.

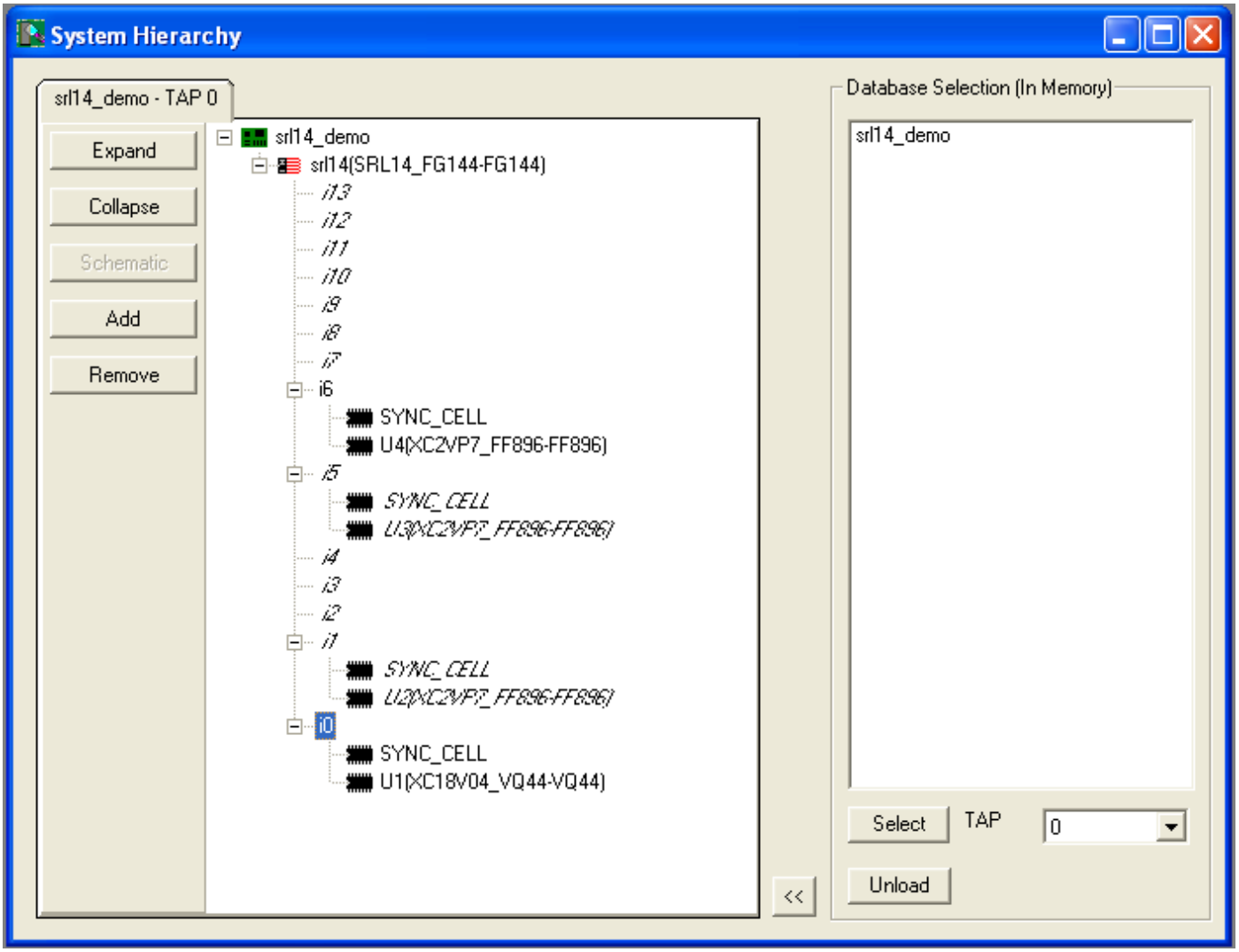


Figure 2: SRL Path Hierarchy Shown in Eclipse

In the DCD file, each secondary scan ring (shown as i13 through i0 in **Error! Reference source not found.**) contains at least one sync cell. The sync cells are placed at the end of

the chain and are defined first, as the link definition begins with the last device or TAP in the scan chain. Following the sync cell, each device in the chain is defined. The definition includes the reference designator, the name of the corresponding BSDL or database, and the type of package, which should be the same as defined within the BSDL or database.

The last device defined within the multi-drop hub is the Scan Ring Linker 14 itself "***srl14***". This should be defined as though it was an additional device on the board or in the system.

Error! Reference source not found. shows the System Hierarchy window from Intellitech's Eclipse Software. This figure, representing the DCD file that Eclipse created, allows the user to turn on and off individual scan chains from within the software.

Ring Select Jumpers

The SRL14 has 4 input pins (SEL[3:0]) that select the single SRL ring that the main TAP controls. Once the ring is selected using the jumpers, the selected ring mirrors the main TAP's TCK, TMS, TDI, TDO, and TRSTN signals. This feature allows a TAP to connect directly to a processor for emulation or to an FPGA for programming or debug. Intellitech's Eclipse or Scan Executive software is required, however, to link together multiple SRL rings to form a single scan chain, useful during any manufacturing test or PCB interconnect test.

All the SEL[3:0] inputs to the SRL14 have weak internal pull-ups. When no jumpers are installed in the system, the select inputs default to all ones, and, as shown in Table 1, no paths are active. To activate a ring, users must tie the necessary SEL inputs to ground, as shown in Table 1.

Active Chain	SEL3	SEL2	SEL1	SEL0
No Rings Active	1	1	1	1
Only Ring 1 Active	1	1	1	0
Only Ring 2 Active	1	1	0	1
Only Ring 3 Active	1	1	0	0

Only Ring 4 Active	1	0	1	1
Only Ring 5 Active	1	0	1	0
Only Ring 6 Active	1	0	0	1
Only Ring 7 Active	1	0	0	0
Only Ring 8 Active	0	1	1	1
Only Ring 9 Active	0	1	1	0
Only Ring 10 Active	0	1	0	1
Only Ring 11 Active	0	1	0	0
Only Ring 12 Active	0	0	1	1
Only Ring 13 Active	0	0	1	0
Only Ring 14 Active	0	0	0	1
All Rings Active	0	0	0	0

Table 1: Ring Select Jumpers Selection

Note:

- While under software control, the SRL14 will ignore the state of the SEL pins.
- When a ring is not active, TMS is driven high.
- When no master is active, TRSTN is driven low. When a master is active, TRSTN is driven to the level of the corresponding TRSTNx input pin.
- TCK and TDI are passed through to all paths.

Pin Descriptions

Power Pins

The SRL14 has 2 independent banks that can operate at different voltages. Please refer to Figure 1 for a high-level diagram of the bank voltages. Bank 1 must be powered at the voltage level of the active controller TAP. Bank 0 must be powered at the voltage level of the TAP interfaces on paths 6 through 14. Acceptable voltages for Bank 0 and 1 are 1.5V, 1.8V, 2.5V or 3.3V. The voltage of each bank is controlled by setting the Vcc_BankX pin for each bank. A description of the power pins for the SRL is listed in Table 2 below.

Pin Name	Pin Number	Description
Vcc_Bank 0	A2, B12, E6, E7, E9, H10	Supply voltage to Bank 0 I/Os Voltages can be 1.5V, 1.8V, 2.5V, or 3.3V
Vcc_Bank 1	E4, J3, L2, L5, L11, M10	Supply voltage to Bank 1 I/Os Voltages can be 1.5V, 1.8V, 2.5V, or 3.3V
Vcc_1.5V	A8, C4, E1, E10, G3, H1, H5, H12, J7	Supply voltage to Core. Nominal 1.5V
Reserved1, Reserved2, Reserved3, Reserved4, Reserved5, Reserved6, Reserved7	J8, J10, L9, L10, L12, M9, M11	Pull down to ground through individual 1KΩresistors
GND	A1, A6, A8, A12, B2, B11, F2, F5, F6, F7, F10, G2, G5, G6, G7, K7, K10, L1, M1, M12	Ground

Table 2: Table of Power Pins

Secondary Scan Rings

Pin Name	Type	Description
TCK_UUT[x]	Output	1149.1 TCK for ring x
TMS_UUT[x]	Output	1149.1 TMS for ring x
TRSTN_UUT[x]	Output	1149.1 TRSTN for ring x
TDO_UUT[x]	Output	1149.1 TDO for ring x. Connects to TDI of first Boundary Scan device in ring x
TDI_UUT[x]	Input	1149.1 TDI from ring x. Connects to TDO of last Boundary Scan device in ring x

Table 3: Table of Secondary Scan Paths

Please refer to Appendix F: 144-Pin FBGA Device Package Pin Assignments for the pin numbers of the Secondary Scan Rings.

Local 1149.1 TAP Interfaces

The 3 local 1149.1 interfaces allow 3 external TAP controllers to access any combination of the 14 secondary scan rings. Designs commonly connect one of these 1149.1 ports to a 10-pin main JTAG header to allow TAP access to external test hardware. Intellitech recommends a 10-pin header configuration for the board layout of the main JTAG interface. The pinout for this configuration is described in Figure 2. In order to provide a controlled impedance of about 100-ohms, and to minimize crosstalk between signals on industry standard ribbon cable, a ground-signal-ground layout is used.

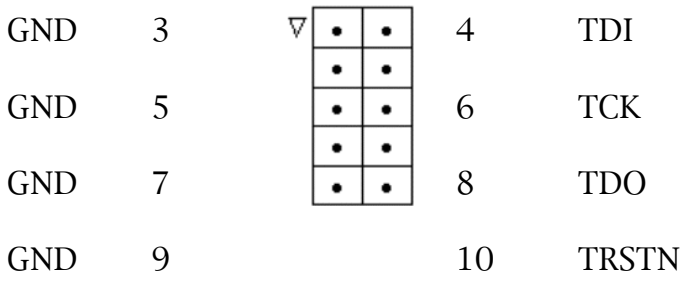


Figure 2: 10-pin Header Pinout

The local 1149.1-compliant TAP interfaces (Master TAPs) are listed in Table 4 through Table 6.

Master TAP 1

Pin Name	Pin #	Type	Description
TCK1	E3	Input	Test Clock. This is the Test Clock for the system under test.
TDI1	F4	Input	Test Data In. Data comes into this port from the TAP controller.
TDO1	G1	Output	Test Data Out. Data goes out of this port to the TAP controller.
TMS1	D3	Input	Test Mode Select. This is the Test Mode Select for the system.
TRST1	D4	Input	Test Reset. This active low input is the Test Reset for the system.

Table 4: Master TAP Interface 1

Master TAP 2

Pin Name	Pin #	Type	Description
TCK2	C3	Input	Test Clock. This is the Test Clock for the system under test.
TDI2	C1	Input	Test Data In. Data comes into this port from the TAP controller.
TDO2	D1	Output	Test Data Out. Data goes out of this port to the TAP controller.
TMS2	C2	Input	Test Mode Select. This is the Test Mode Select for the system.
TRSTN2	D2	Input	Test Reset. This active low input is the Test Reset for the system.

Table 5: Master TAP Interface 2

Master TAP 3

Pin Name	Pin #	Type	Description
TCK3	H4	Input	Test Clock. This is the Test Clock for the system under test.
TDI3	H2	Input	Test Data In. Data comes into this port from the TAP controller.
TDO3	F1	Output	Test Data Out. Data goes out of this port to the TAP controller.
TMS3	E2	Input	Test Mode Select. This is the Test Mode Select for the system.
TRSTN3	F3	Input	Test Reset. This active low input is the Test Reset for the system.

Table 6: Master TAP Interface 3

DC and Switching Characteristics

Operating Conditions

Refer to Table 7 for the absolute maximum rated conditions. Stress beyond these limits may cause permanent damage. Exposure to these conditions for an extended period of time may affect the SB1AC1 device reliability. This device should be not operated outside the recommended operating ranges specified in Table 10.

Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCCCORE	DC core supply voltage	-0.3 to 1.65	V
VCCIO	DC I/O supply voltage	-0.3 to 3.75	V
$T_{STORAGE}$	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+125 (+150[1])	°C

Table 7: Absolute Maximum Ratings

Notes 1) Automotive Junction Temperature Max

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	Max, V	Min,V	Max, V	Max, V	Min,V	mA	mA
-0.3	0.8	2	3.6	0.4	2.4	12	12

Table 8: Maximum and Minimum DC Input/Output Levels

Drive Strength - 12mA

Note: Applicable to both Industrial and Commercial Conditions

Commercial		Industrial		Units
I_{IL}	I_{IH}	I_{IL}	I_{IH}	
10	10	15	15	uA

Table 9: Maximum and Minimum DC Input Levels

Note: Commercial Range (0° < T_A < 70° C) , Industrial Range (-40° < T_A < 85° C)

Recommended Operating Conditions

Symbol	Parameter	Range	Units
VCC_1.5V	1.5V DC core supply voltage	1.425 to 1.575	V
VCC_Bank0	Bank 0 I/O supply voltage	1.5 to 3.6	V
VCC_Bank1	Bank 1 I/O supply voltage	1.5 to 3.6	V
T_A	Ambient Temperature	0 to +70 Com / -40 to +85 Ind	°C
T_J	Junction Temperature	0 to +85 Com / -40 to +100 Ind	°C
T_{j1}	Junction Temperature Automotive Grade 1	-40 to +135	°C
T_{j2}	Junction Temperature Automotive Grade 2	-40 to +115	°C

Table 10: Recommended Operating Conditions

Quiescent Supply Current

	Maximum	Units
Commercial	10	mA
Industrial	15	mA

Table 11: Quiescent Supply Current

Power Consumption

Minimum	Nominal	Maximum	Units
3.9	4.2	11.6	mA

Table 12: Current Draw on VCC_1.5V

Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C.

Package Thermal Resistivities

Package	Pin Count	θ_{jc}	θ_{ja} – Still Air	θ_{ja} – 200 ft./min.	θ_{ja} – 500 ft./min.	Units
FBGA	144	3.8	26.9	22.9	21.5	C/W

Table 13: Package Thermal Resistivities

Temperature and Voltage De-rating Factors for Timing Delays

(Normalized to T_J = 70°C, V_{CC} = 1.425 V)

Array Voltage V_{cc} (V)	-40°C	0°C	25°C	70°C	85°C	110°C
1.425	0.87	0.92	0.95	1.00	1.02	1.05
1.500	0.83	0.88	0.90	0.95	0.97	0.99
1.575	0.80	0.85	0.87	0.2	0.93	0.96

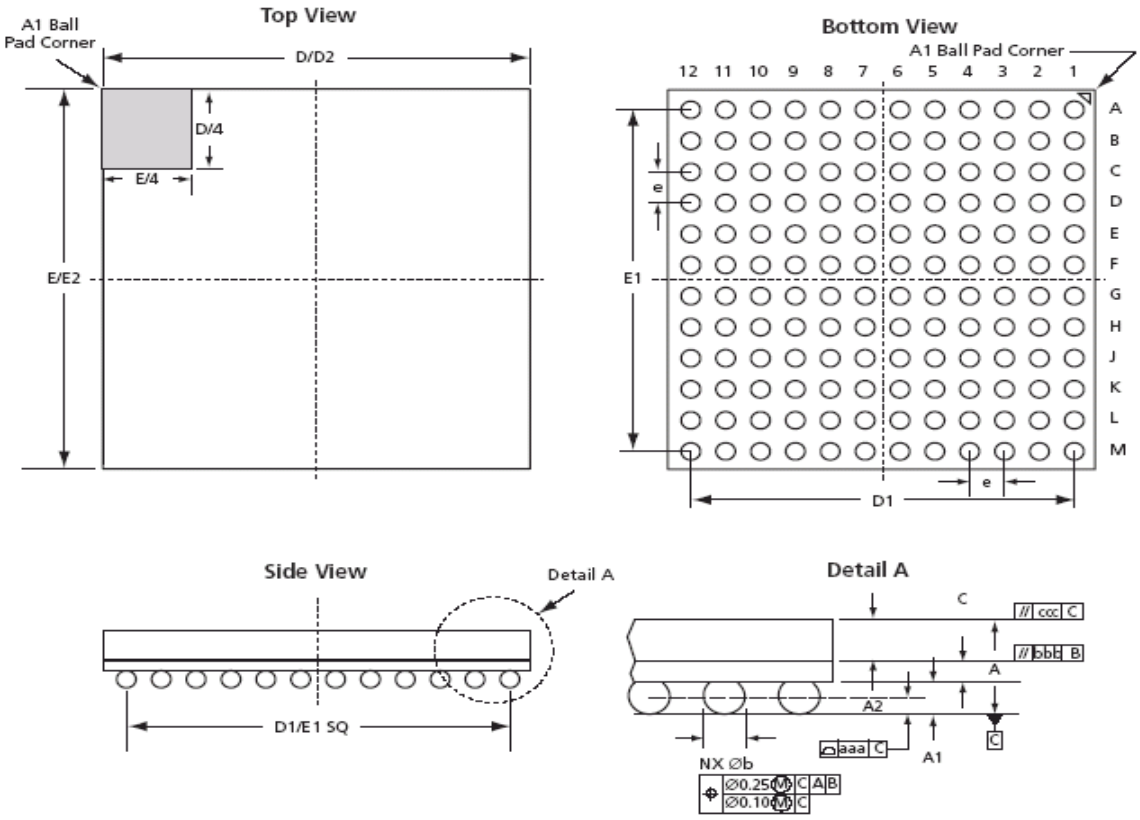
Table 14: Temperature and Voltage Derating Factors for Timing Delays for non Automotive parts

Array Voltage V_{cc} (V)	-40°C	0°C	25°C	70°C	85°C	115°C	125°C	135°C
1.425	0.83	0.88	0.90	0.95	0.97	1.00	1.01	1.02
1.500	0.79	0.83	0.85	0.90	0.92	0.95	0.96	0.97
1.575	0.76	0.80	0.82	0.87	0.88	0.91	0.93	.094

Table 15: Temperature and Voltage Derating Factors for Timing Delays for Automotive parts

Appendix A: Device Package Information

144-Pin FBGA



Dimension	Min.	Nom.	Max.
A	1.35	1.45	1.55
A1	0.35	0.40	0.45

A2	0.65	0.70	0.75
aaa	0.12	0.12	0.12
b	0.45	0.50	0.55
bbb	0.25	0.25	0.25
c	0.35	0.35	0.35
ccc	0.35	0.35	0.35
D	12.80	13.00	13.20
D1	11.00 BSC	11.00 BSC	11.00 BSC
D2	12.80	13.00	13.20
E	12.80	13.00	13.20
E1	11.00 BSC	11.00 BSC	11.00 BSC
E2	12.80	13.00	13.20
e	1.00 typ.	1.00 typ.	1.00 typ.

Table 16: FBGA Array Dimensions

Notes: 1) All dimensions are in millimeters. 2) BSC – Basic Spacing between Centers

Appendix B: Package Chemical Content

SRL14-144 ROHS6 (Lead–Free)

Lead Finish	100% Matte Tin
Tin Whisker Mitigation	105°C Bake, 1hr
Package Peak Reflow Temp	260°C
Time Within 50°C of Actual Peak Temp (s)	20-40
ROHS Compliance	YES
Compatible with SnPb solder	YES
Lead-Pb (ppm)	<1,000
Mercury –Hg (ppm)	<1,000
Cadmium-Cd (ppm)	<100
Hexavalent Chromium Cr(VI) (ppm)	<1,000
Polybrominated Diphenyl Ethers - PBDE (ppm)	0
Polybrominated Biphenyls – PPB (ppm)	0

SRL14-144 ROHS5

Lead Finish	85% Sn / 15% Pb

Tin Whisker Mitigation	N/A
Package Peak Reflow Temp	225 +0/-5
Time Within 5°C of Actual Peak Temp (s)	10-30
ROHS Compliance	YES
Compatible with Lead Free Reflow	NO
Lead-Pb (ppm)	>1,000
Mercury –Hg(ppm)	<1,000
Cadmium-Cd (ppm)	<100
Hexavalent Chromium Cr(VI) (ppm)	<1,000
Polybrominated Diphenyl Ethers - PBDE (ppm)	0
Polybrominated Biphenyls – PPB (ppm)	0

Appendix C: DC and Switching Characteristics

Operating Conditions

Refer to Table 17 for the absolute maximum rated conditions. Stress beyond these limits may cause permanent damage. Exposure to these conditions for an extended period of time may affect the SRL14 device reliability. This device should not be operated outside the recommended operating ranges specified in Table 18.

Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCCCORE	DC core supply voltage	-0.3 to 1.65	V
VCCIO	DC I/O supply voltage	-0.3 to 3.75	V
$T_{STORAGE}$	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+125 (+150[1])	°C

Table 17: Absolute Maximum Ratings

Notes: 1) Automotive Junction Temperature Max

Recommended Operating Conditions

Symbol	Parameter	Range	Units
VCCCORE	1.5V DC core supply voltage	1.425 to 1.575	V
VCCIO	3.3V DC I/O supply voltage	3.0 to 3.6	V
T_A	Ambient Temperature	0 to +70 Com / -40 to +85 Ind	°C
T_J	Junction Temperature	0 to +70 Com / -40 to +85 Ind	°C

T_{j1}	Junction Temperature Automotive Grade 1	-40 to +135	°C
T_{j2}	Junction Temperature Automotive Grade 2	-40 to +115	°C

Table 18: Recommended Operating Conditions

Summary of I/O DC Input and Output levels

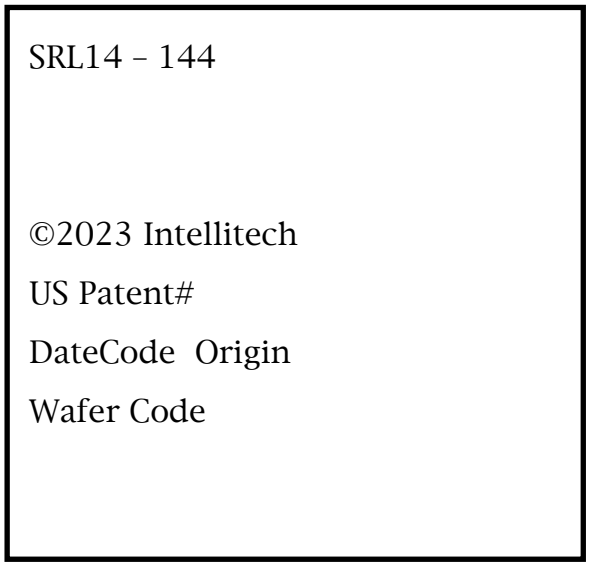
I/O standard	Drive Strength	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		Min, V	Max, V	Min, V	Max, V	Max,V	Min,V	mA	mA
3.3v	12mA	-0.3	0.8	2	3.6	0.4	2.4	12	12
2.5v	12mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8v	8 mA	-0.3	$0.35*V_{CCI}$	$0.65*V_{CCI}$	3.6	0.45	V_{CCI}-0.45	8	8
1.5v	4 mA	-0.3	$0.30*V_{CCI}$	$0.70*V_{CCI}$	3.6	$0.25*V_{CCI}$	$0.75*V_{CCI}$	4	4

Table 19: I/0 DC Input and Output Levels

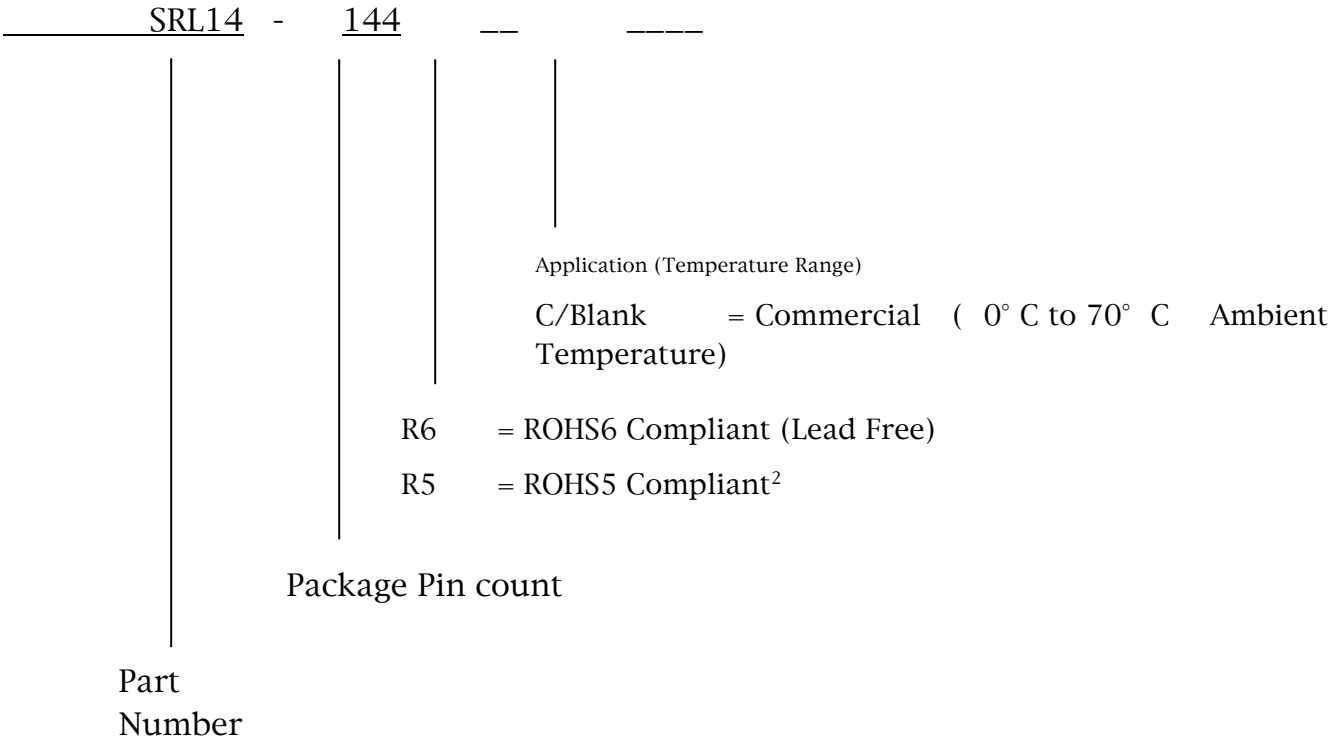
Notes:

Currents are measured at 85 degrees Celsius junction temperature

Appendix D: Device Package Markings



Appendix E: Device Ordering Information



Notes:

1) Industrial and Automotive grade components are available through special order only. Lead times may be extended

2) ROHS 5 compliant parts are available through special order only. Lead times may be extended.

Appendix F: 144-Pin FBGA Device Package Pin Assignments

Power Pins

Pin Number	Function
A1	GND
A6	GND
A8	Vcc_1.5V
A12	GND
B2	GND
B11	GND
C4	Vcc_1.5V
E1	Vcc_1.5V
E10	Vcc_1.5V
F2	GND
F5	GND
F6	GND
F7	GND
F10	GND
G2	GND
G3	Vcc_1.5V
G5	GND
G6	GND
G7	GND
H1	Vcc_1.5V
H5	Vcc_1.5V
H12	Vcc_1.5V
J7	Vcc_1.5V
J8	Reserved1
J10	Reserved2
K7	GND
K10	GND
L1	GND
L9	Reserved3
L10	Reserved4
L12	Reserved5
M1	GND
M8	N/C
M9	Reserved6
M11	Reserved7
M12	GND

Bank 0 Pins

Pin Number	Function
A2	Vcc_Bank0
A3	TMS_UUT[9]
A4	TDI_UUT[10]
A5	TDO_UUT[11]
A7	TMS_UUT[10]
A9	TDO_UUT[12]
A10	TDI_UUT[13]
A11	TMS_UUT[13]
B3	TRSTN_UUT[9]
B4	TCK_UUT[10]
B5	TRSTN_UUT[1
	1]
B6	TCK_UUT[11]
B7	TDI_UUT[12]
B8	TCK_UUT[12]
B9	TMS_UUT[12]
B10	TCK_UUT[13]
B12	Vcc_Bank0

C5	TMS_UUT[11]
C6	TDI_UUT[11]
C7	TRSTN_UUT[8]
C8	TMS_UUT[8]
C9	TRSTN_UUT[12]
C10	TDO_UUT[13]
C11	TDI_UUT[9]
C12	SEL[0]
D5	TRSTN_UUT[10]
D6	TCK_UUT[9]
D7	TDO_UUT[8]
D8	TDO_UUT[10]
D9	TDO_UUT[9]

D10	TRSTN_UUT[13]
D11	SEL[3]
D12	SEL[2]
E6	Vcc_Bank0
E7	Vcc_Bank0
E8	TMS_UUT[7]
E9	Vcc_Bank0
E11	TRSTN_UUT[6]
E12	SEL[1]
F8	TCK_UUT[8]
F9	TCK_UUT[7]
F11	TMS_UUT[6]
F12	TDI_UUT[6]
G8	TDI_UUT[8]

G9	TDO_UUT[7]
G10	TDI_UUT[7]
G11	TDO_UUT[6]
G12	TCK_UUT[6]
H6	SELECTED_L
H9	TRSTN_UUT[7]
H10	Vcc_Bank0
H11	TCK_UUT[5]
J11	TDO_UUT[5]
J12	TDI_UUT[5]
K11	TRSTN_UUT[5]
K12	TMS_UUT[5]

Bank 1 Pins

Pin Number	Function
B1	N/C
C1	TDI2
C2	TMS2
C3	TCK2
D1	TDO2
D2	TRSTN2
D3	TMS11
D4	TRSTN1
E2	TMS3
E3	TCK1
E4	Vcc_Bank1
E5	BASE_ADDR[1]
F1	TDO3
F3	TRSTN3
F4	TDI1
G1	TDO1
G4	CONCURRENT MASK
H2	TDI3
H3	CONCURRENT EXP DATA
H4	TCK3
H8	TDO_UUT[3]
J1	TMS_UUT[0]
J2	TDI_UUT[0]
J3	VCC Bank 1
J4	TCK_UUT[2]
J5	TMS_UUT[2]
J6	TCK_UUT[3]
J9	BASE_ADDR[0]
K1	TRSTN_UUT[0]
K2	TCK_UUT[0]
K3	TRSTN_UUT[1]
K4	TRSTN_UUT[2]
K5	TDO_UUT[2]
K6	TDI_UUT[3]
K8	TMS_UUT[4]
K9	TRSTN_UUT[4]
L2	VCC Bank1
L3	TDI_UUT[1]
L4	TMS_UUT[1]
L5	VCC Bank 1
L6	TMS_UUT[3]
L7	TDO_UUT[4]
L8	TDI_UUT[4]
L11	VCC Bank 1
M2	TDO_UUT[0]
M3	TCK_UUT[1]
M4	TDO_UUT[1]
M5	TDI_UUT[2]
M6	TRSTN_UUT[3]
M7	TCK_UUT[4]
M10	VCC Bank 1

Appendix G: Example DCD File with SRL14

```
! Device Chain Description file (.dcd) for SRL14
version 2;
! Define hub
hub srl14;

! Define the specific type of hub (SRL)
   type = srl;

   ssp i13;
   end ssp;

   ssp i12;
   end ssp;

   ssp i11;
   end ssp;

   ssp i10;
   end ssp;

   ssp i9;
   end ssp;

   ssp i8;
   end ssp;

   ssp i7;
   end ssp;
```

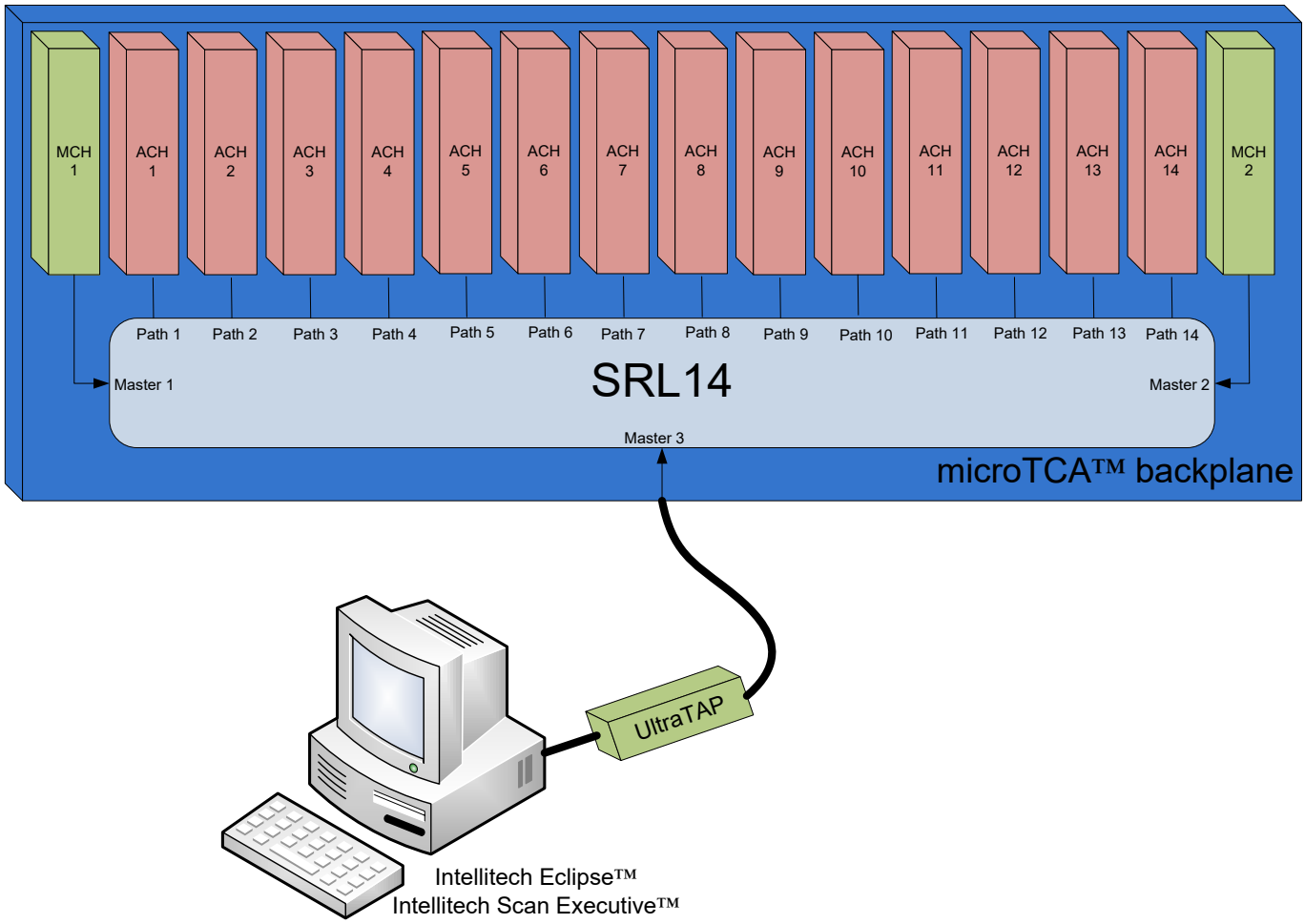


```
  ssp i6;
    sync_cell;
    device U4 xilinx$virtex_ii_pro$xc2vp7$ff896 ff896;
  end ssp;

  ssp i5;
    sync_cell;
    device U3 xilinx$virtex_ii_pro$xc2vp7$ff896 ff896;
  end ssp;

  ssp i4;
  end ssp;

  ssp i3;
  end ssp;

  ssp i2;
  end ssp;

  ssp i1;
    sync_cell;
    device U2 xilinx$virtex_ii_pro$xc2vp7$ff896 ff896;
  end ssp;

  ssp i0;
    sync_cell;
    device U1 xilinx$xc18v00$xc18v04$vq44 vq44;
  end ssp;
```

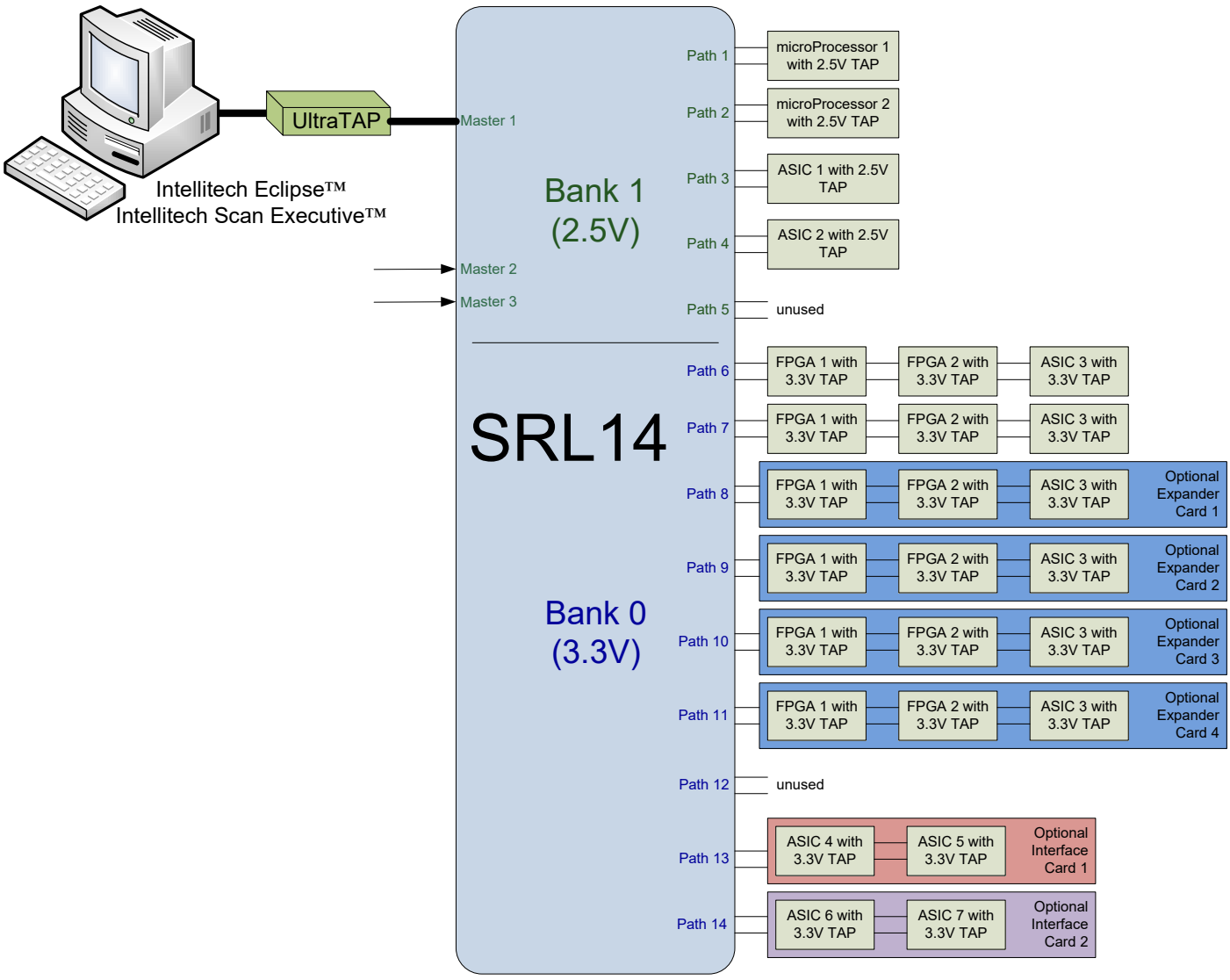


```
  device srl14 srl14_fg144 FG144;

end hub;
```

Appendix H: Use of SRL14 in Test of MicroTCA™ System



Appendix I: Use of SRL14 in a Multi-Voltage System



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